LAr TPC Progress at BNL

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BROOKHAVEN NATIONAL LABORATORY

DOE OHEP Site Visit
September 11, 2012

LAr TPC Work at BNL

Cryogenics, TPC, Cold Electronics ⟷ LAr Detector R&D, MicroBooNE, LarLAr, LBNE FD

MicroBooNE

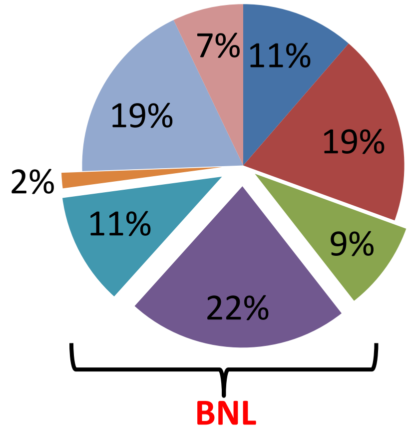
Craig Thorn is Deputy Project Manager for Active Detector

Sue Duffin is L2 manager for Cryostat ($1.4M, 9%)

Bo Yu is co-convener of Active Detector TPC subsystem, in charge of TPC design ($3.6M, 22%) (L2 is at Yale)

Hucheng Chen is L2 manager for Readout & DAQ ($1.8M, 11%)

George Mahler is L2 Manager for Detector Design and Construction Integration ($0.25M, 2%)



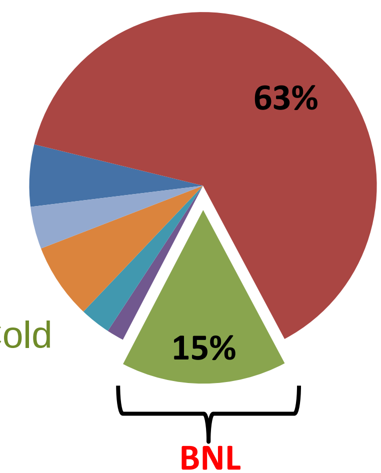
LBNE Project management:

Mary Bishai	Project Scientist
Penka Novakova	Controls Specialist
Jeff Dolph	Project Engineer
Milind Diwan	Collaboration Co-Spokesperson
Jim Stewart	L2 Manager for FD

LBNE LArTPC

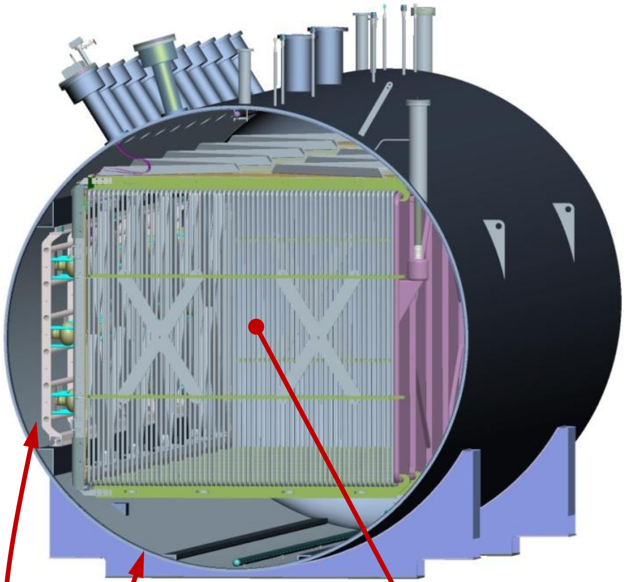
Bo Yu is L3 manager for TPC (~10% of BCWS)

Craig Thorn is L3 manager for Cold Electronics (~5% of BCWS)



Work done in collaboration with SMU, GIT, MSU, Yale, Princeton, MIT, Syracuse, U. Penn, U. Wisconsin

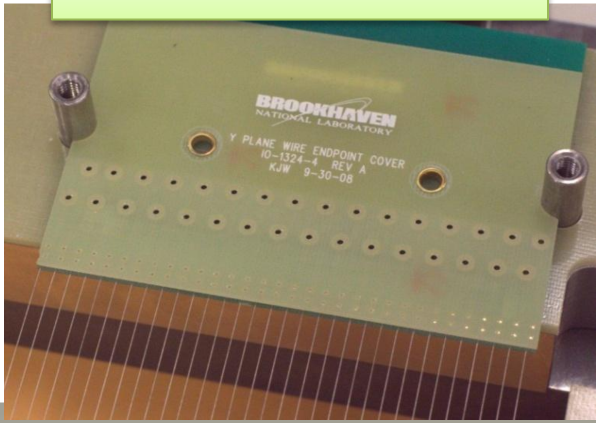
Main Elements of the MicroBooNE Detector

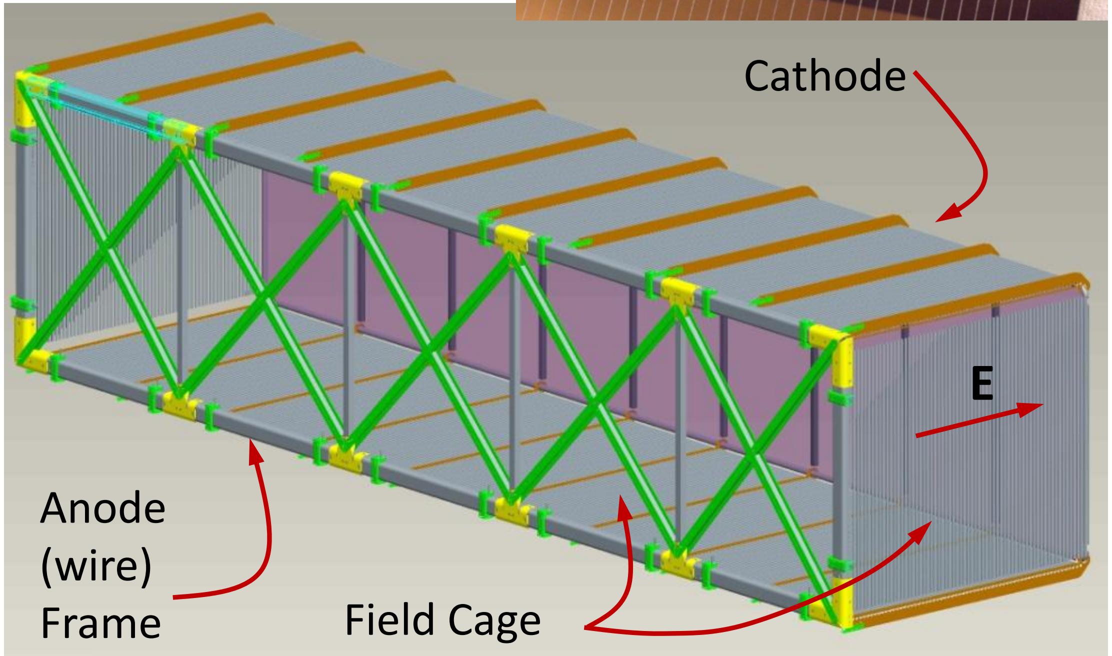


Cryostat with TPC and PMT detectors

Cryostat, TPC, cold electronics and detector assembly and integration are BNL responsibilities

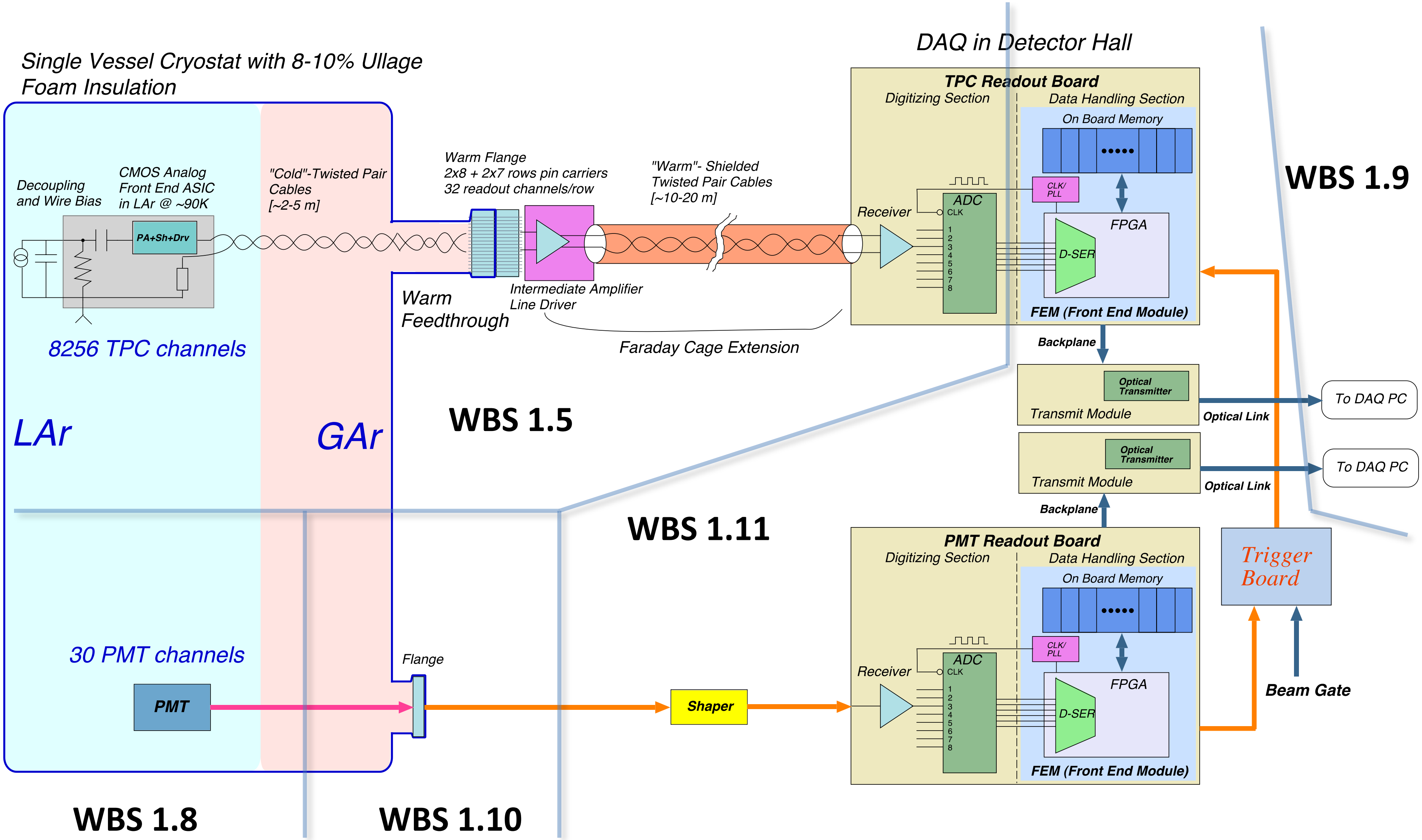
32 wire carrier board



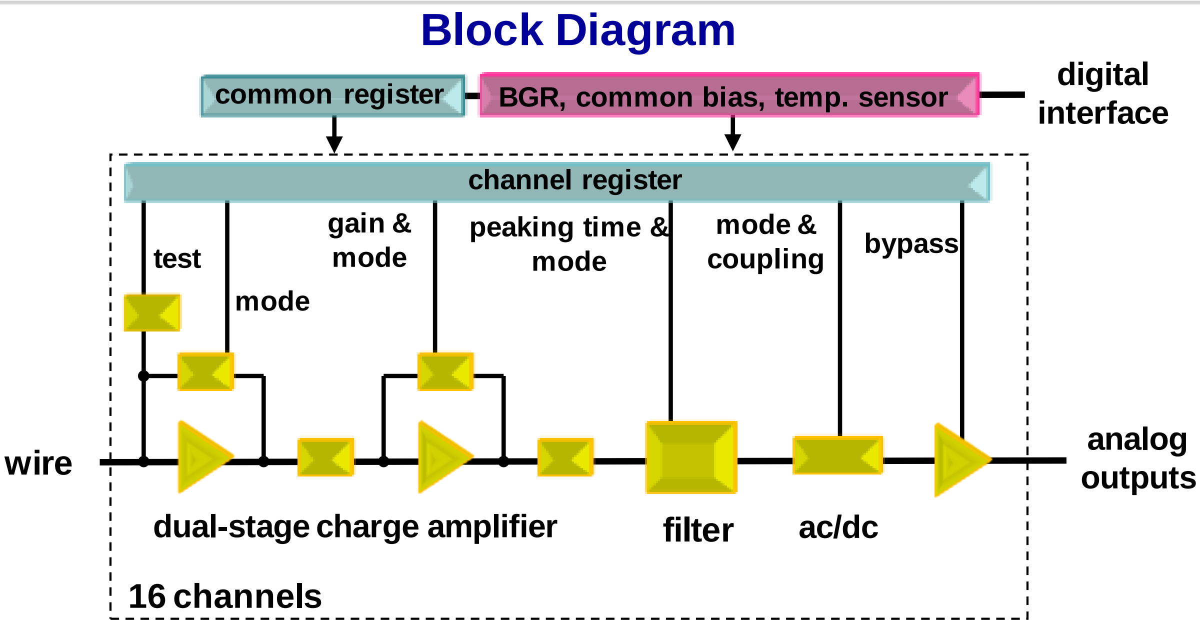


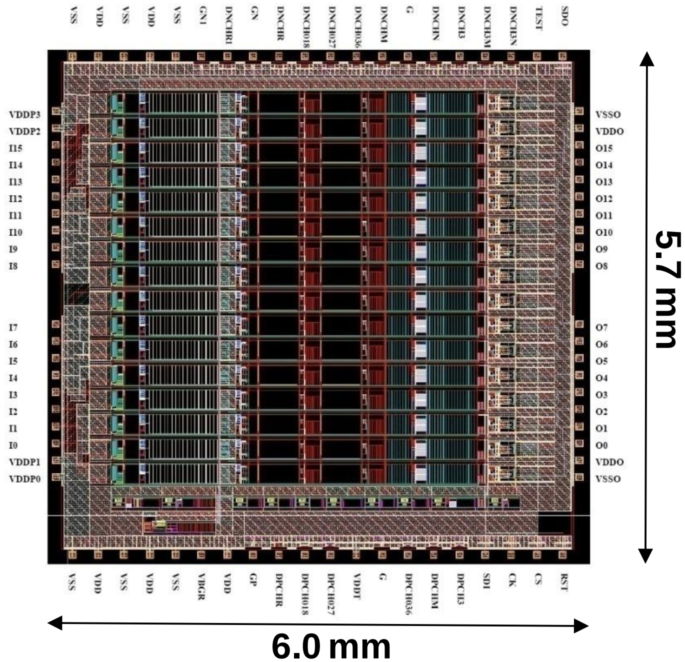
3 wire planes (Y, U, V)
8256 wires
3 mm wire/plane spacing
2.5 m drift (125kV HV)
8’ x 8’ x 35’, 170t LAr

MicroBooNE Electronics System Overview



Analog Front-End (FE) ASIC for MicroBooNE and LBNE FD





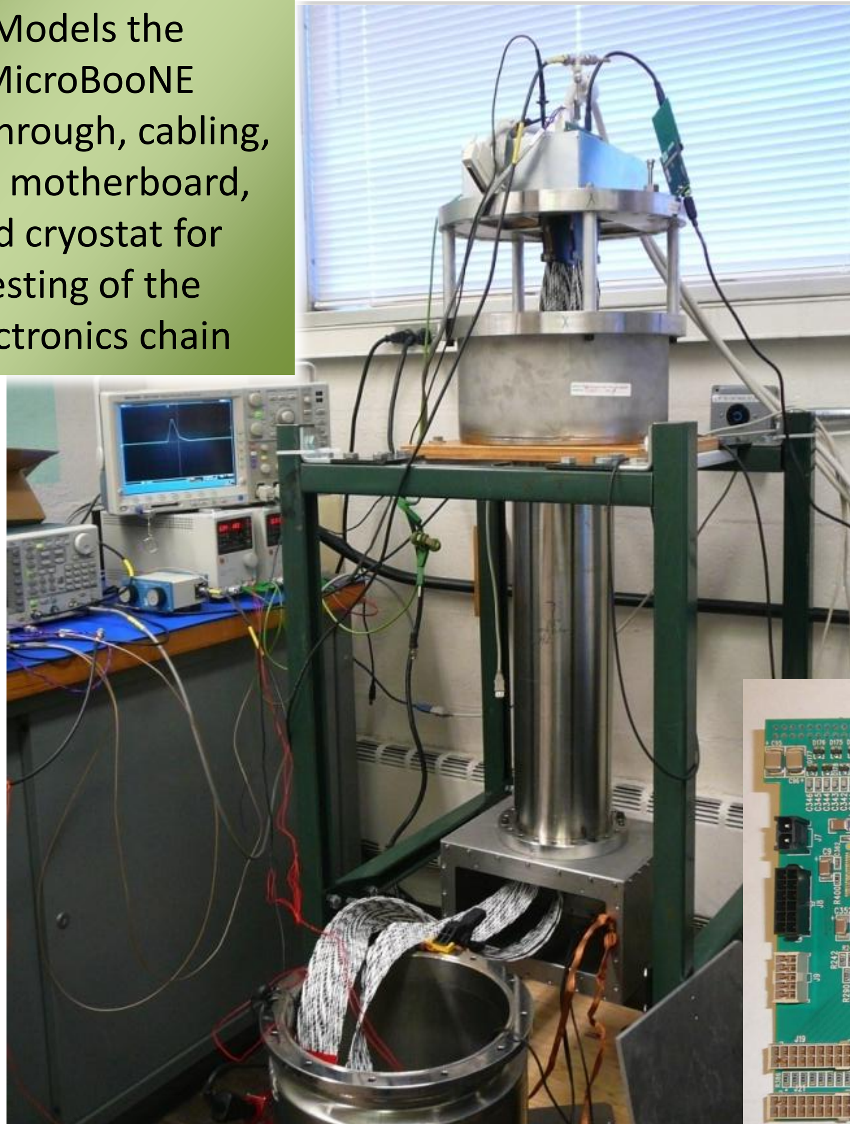
- 16 channels
- charge amplifier, high-order anti-aliasing filter
- programmable gain: 4.7, 7.8, 14, 25 mV/fC
  (charge 55, 100, 180, 300 fC)
- programmable filter
  (peaking time 0.5, 1, 2, 3 μs)
- programmable collection/non-collection mode
  (baseline 200, 800 mV)
- programmable dc/ac coupling (100μs)

- technology CMOS 0.18 μm, 1.8 V,
- **designed for room and cryogenic operation**
- 136 programming registers with digital interface
- 5.5 mW/channel (input MOSFET 3.9 mW)
- single MOSFET test structures
- ~ 15,000 MOSFETs

Thermal Cycling of FE ASICs and FE boards for MicroBooNE

Test setup for assembled FE boards

Models the MicroBooNE feedthrough, cabling, ASIC motherboard, and cryostat for testing of the electronics chain

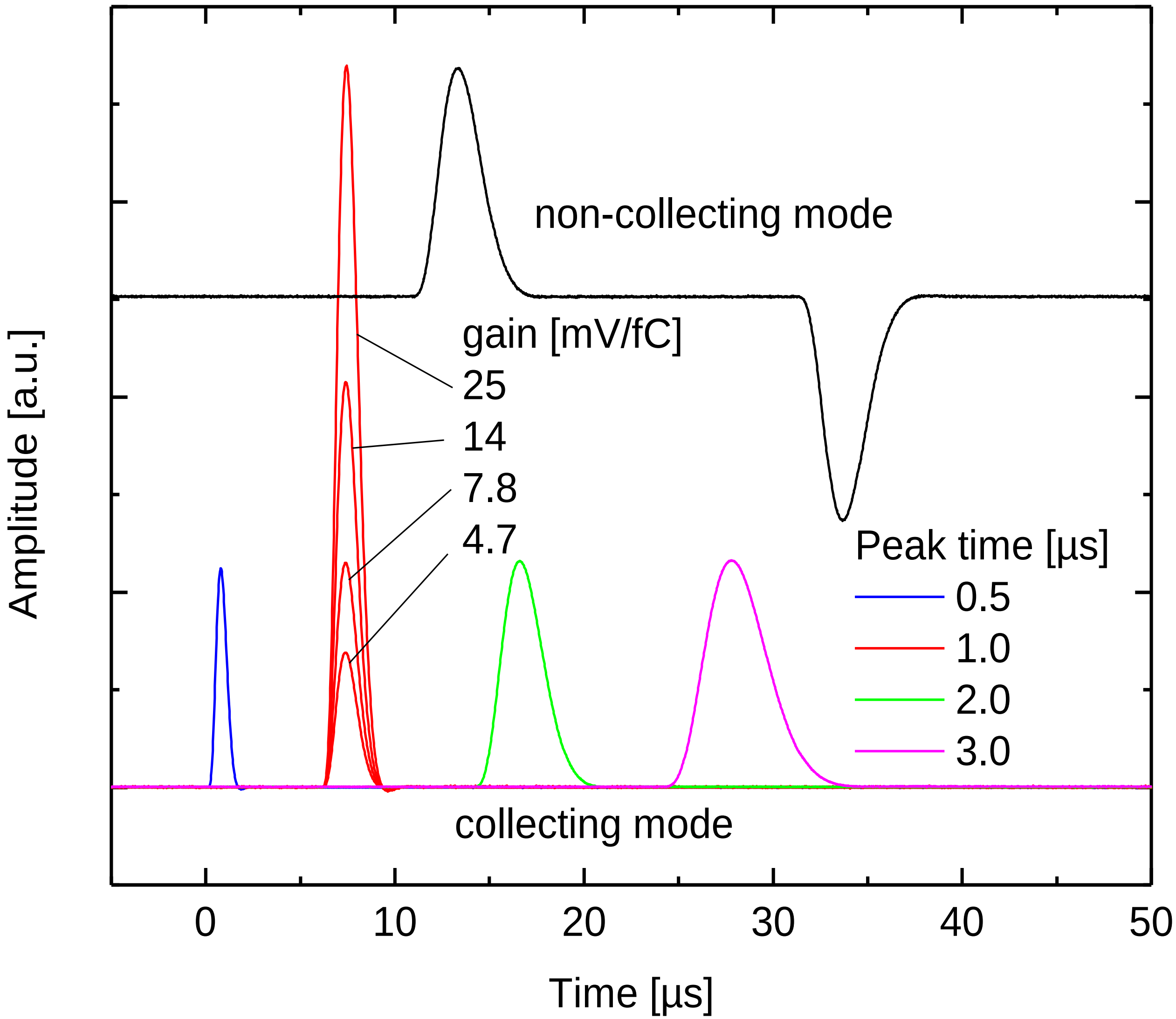


The ASICs have been extensively tested both warm and in LN2. The chip yield for both is >90%.

The ASICs and the motherboard have experienced >1000 chip immersions in LN_2,

Cold Mother Board with 12 ASICs populated (192 channels)

Signal Measurements:
Programmable Gain, Peak Time and Baseline



Bandgap Reference:

$$V_{BGR} \approx \begin{cases} 1.185\ \text{V} & \text{at } 300\ °\text{K} \\ 1.164\ \text{V} & \text{at } 77\ °\text{K} \end{cases}$$

variation ≈ 1.8 %

Temperature Sensor:

$$V_{TMP} \approx \begin{cases} 867.0\ \text{mV} & \text{at } 300\ °\text{K} \\ 259.3\ \text{mV} & \text{at } 77\ °\text{K} \end{cases}$$

~ 2.86 mV / °K

Programmable gain, peaking time and baseline

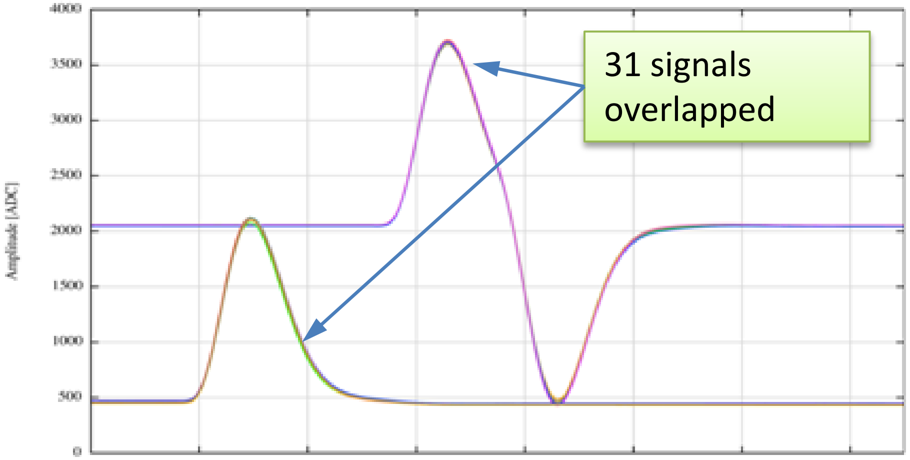
Maximum charge of 55, 100, 180, or 300 fC

Analog ASIC Gain and Waveform Uniformity

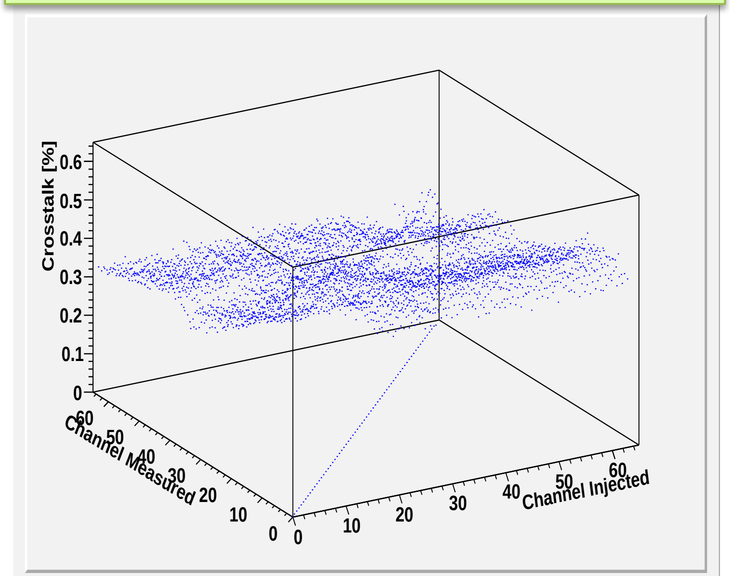
Measurements for ASICs on MicroBooNE Motherboard

Residuals from a linear fit < 0.3%
Crosstalk < 0.3%

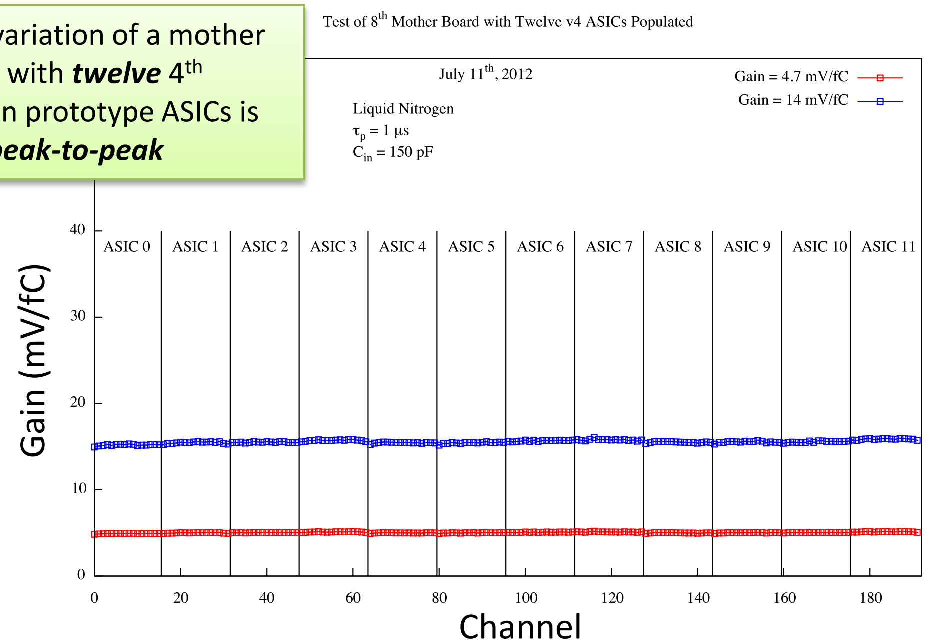
These measurements were performed with the entire MicroBooNE signal chain:
Analog ASIC + cold cable + intermediate amplifier + ADC



Measured Crosstalk < 0.3%

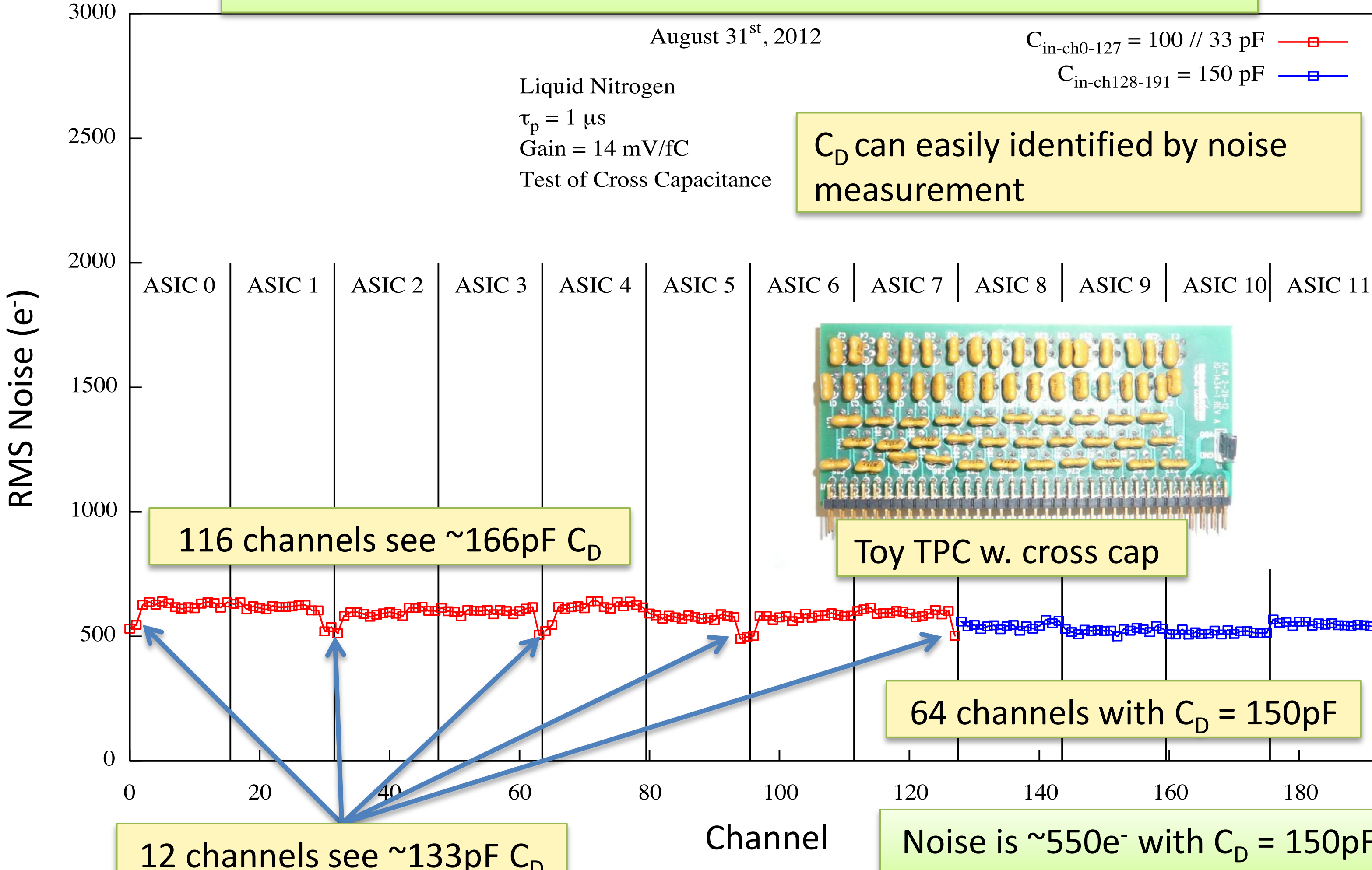


Gain variation of a mother board with ***twelve*** 4th version prototype ASICs is ~7% ***peak-to-peak***



Measurements for FE ASICs on MicroBooNE Motherboard

Test of 12th Mother Board in LN2 with 12 ASICs Populated (192 channels)



Noise is ~550e^- with C_D = 150pF in LN_2

CMOS FE ASIC Summary

- The LBNE CMOS FE ASIC is being used for the MicroBooNE Project
- The ASIC has been tested systematically on the mother board in the MicroBooNE FE test stand
- 1400 chips are in fabrication, delivery by 11/15/2012
- Excellent performance
    - Noise <600 e- at 77K and 220pF
    - Channel-to-channel and chip-to-chip gain, calibration, shaping,… variations are small
    - Crosstalk <1%
    - Properties (except noise) identical at room temperature and in LN2
- This FE ASIC will be used with the ADC under development and a cold FPGA for the 35t prototyping

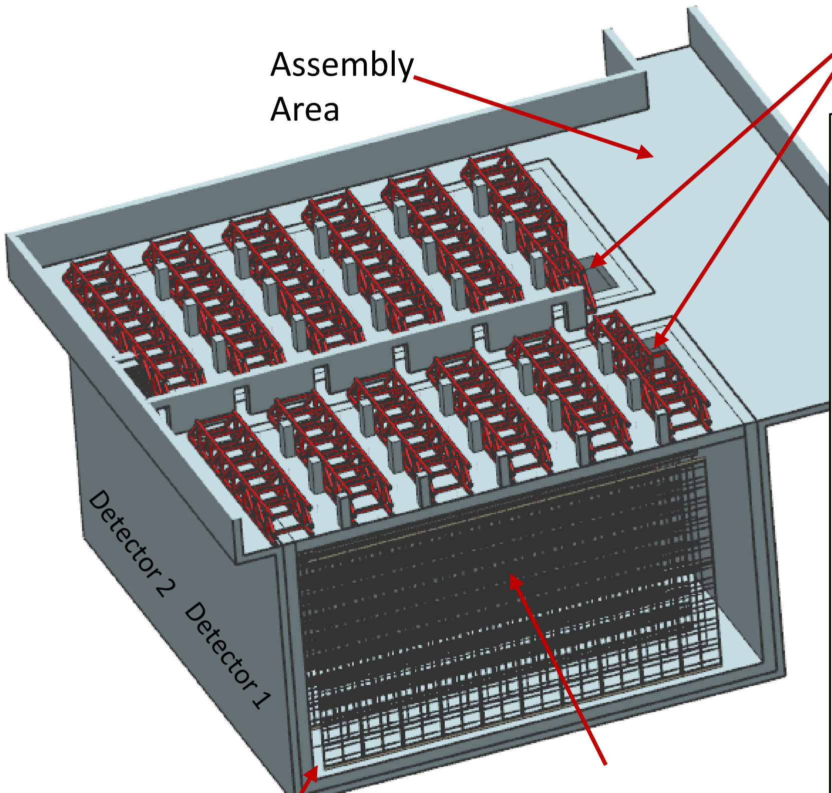
LBNE Far Detector - LArTPC

BNL responsibility:

TPC Structure

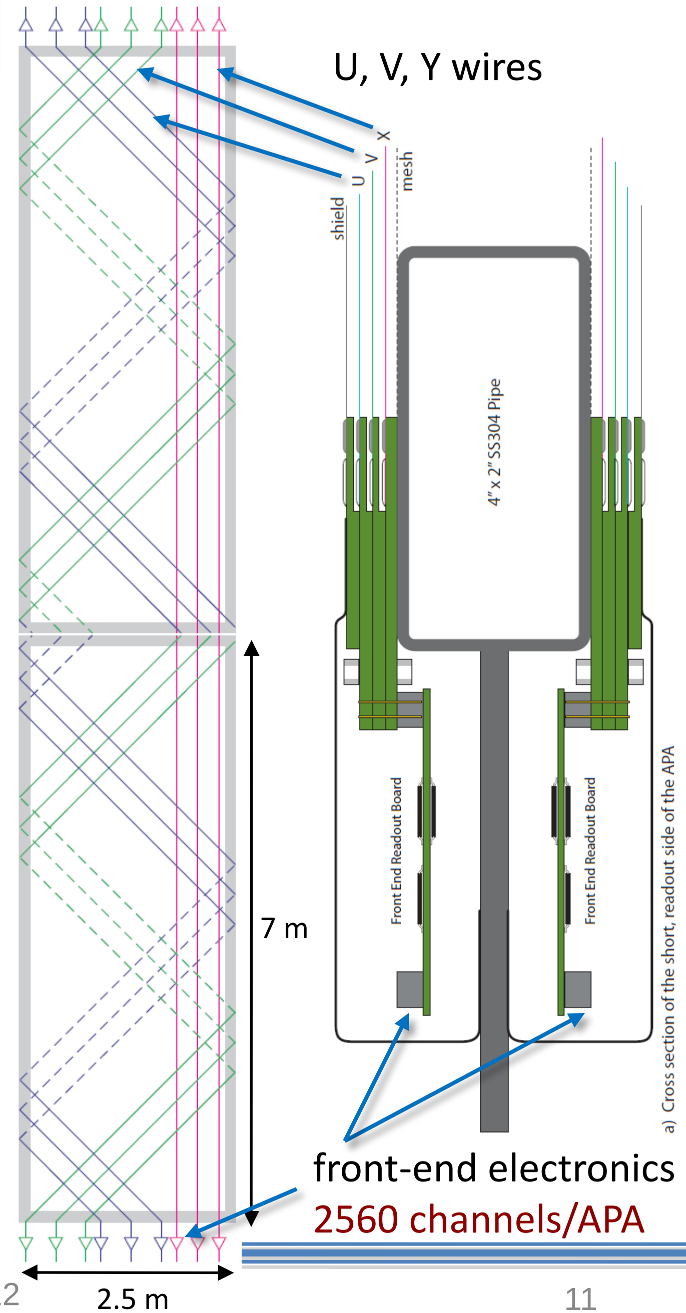
- Anode Plane Assembly (APA)
- Cathode Plane Assembly (CPA)

Cold Electronics (in LAr)



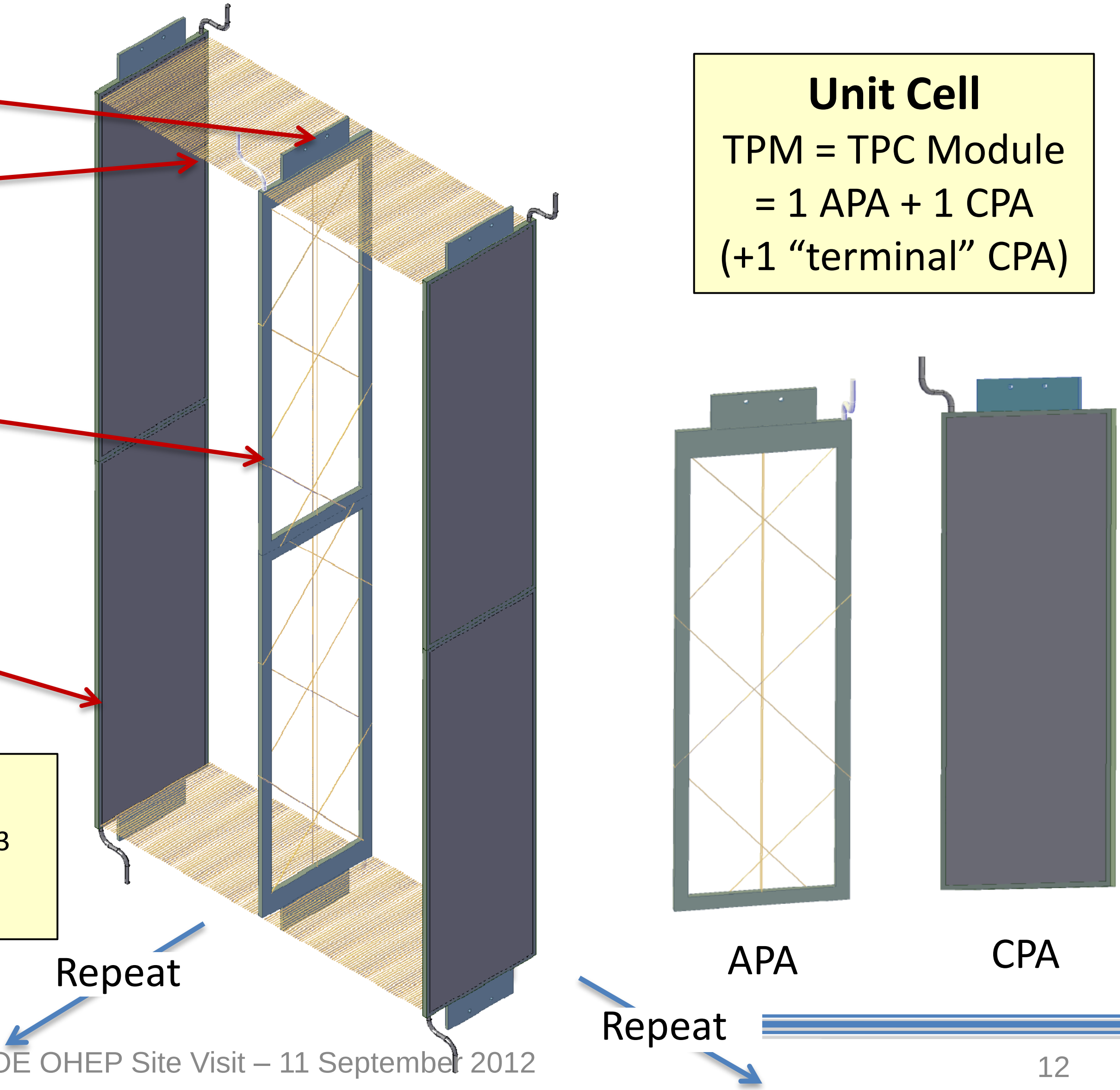
307,200 channels total

APAs are structural & electrical units, containing all sense wires and ***cold readout electronics***. This subsystem also includes all cabling inside the cryostat, electronics power and wire bias supplies, and electronics feedthroughs.



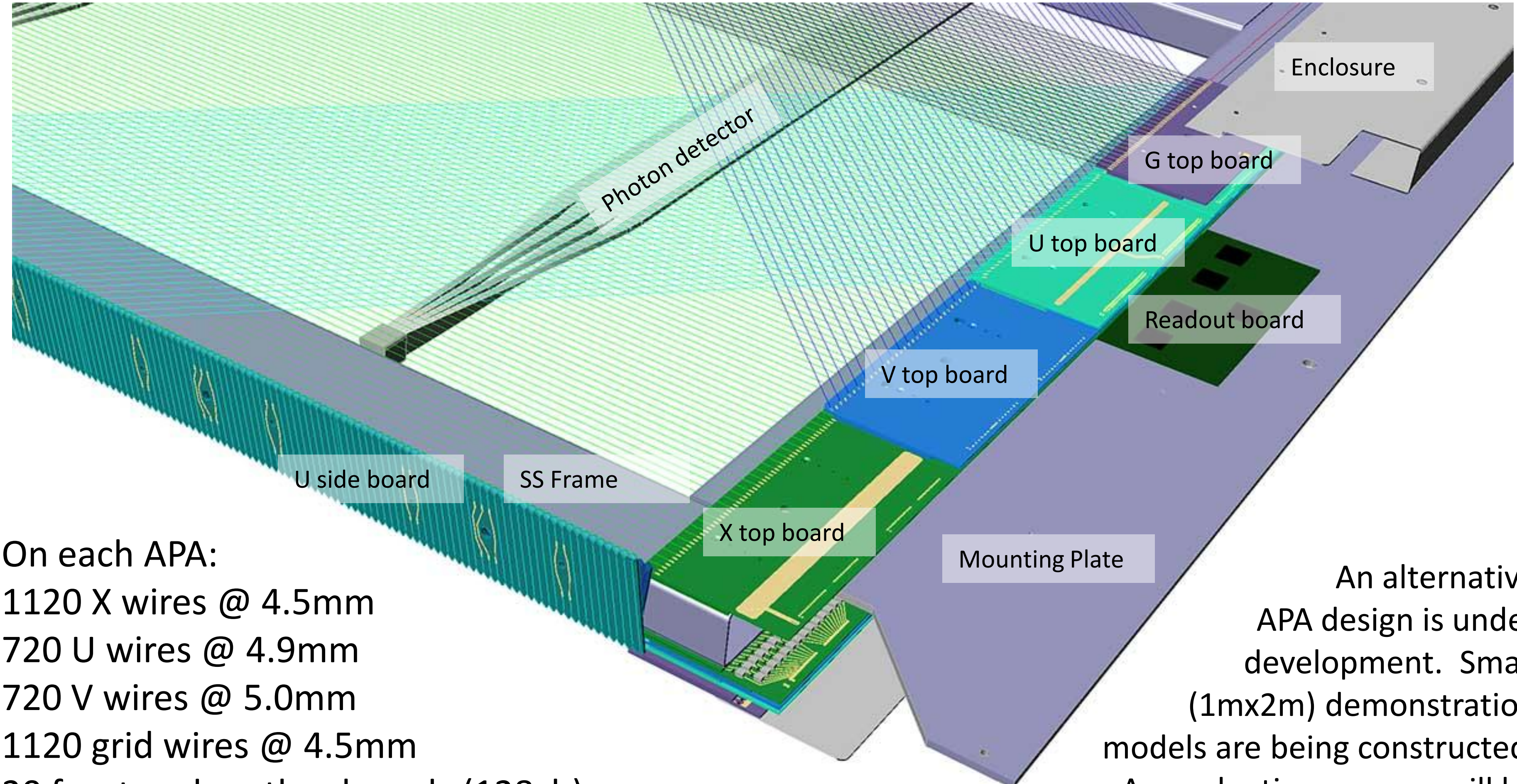
APA + CPA Assemblies form TPC Modules
in a Large Cryostat

Unit Cell
TPM = TPC Module
= 1 APA + 1 CPA
(+1 “terminal” CPA)



Active volume/APA
2 x 2.5m x 7m x 3.8m=130 m^3
= 181 ton

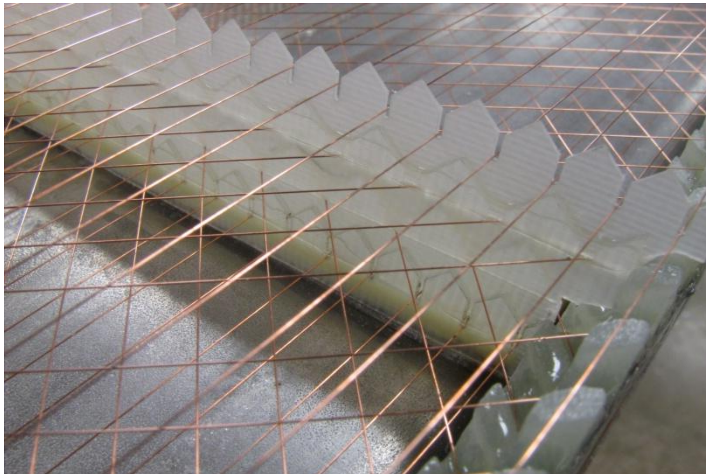
APA Close-up View

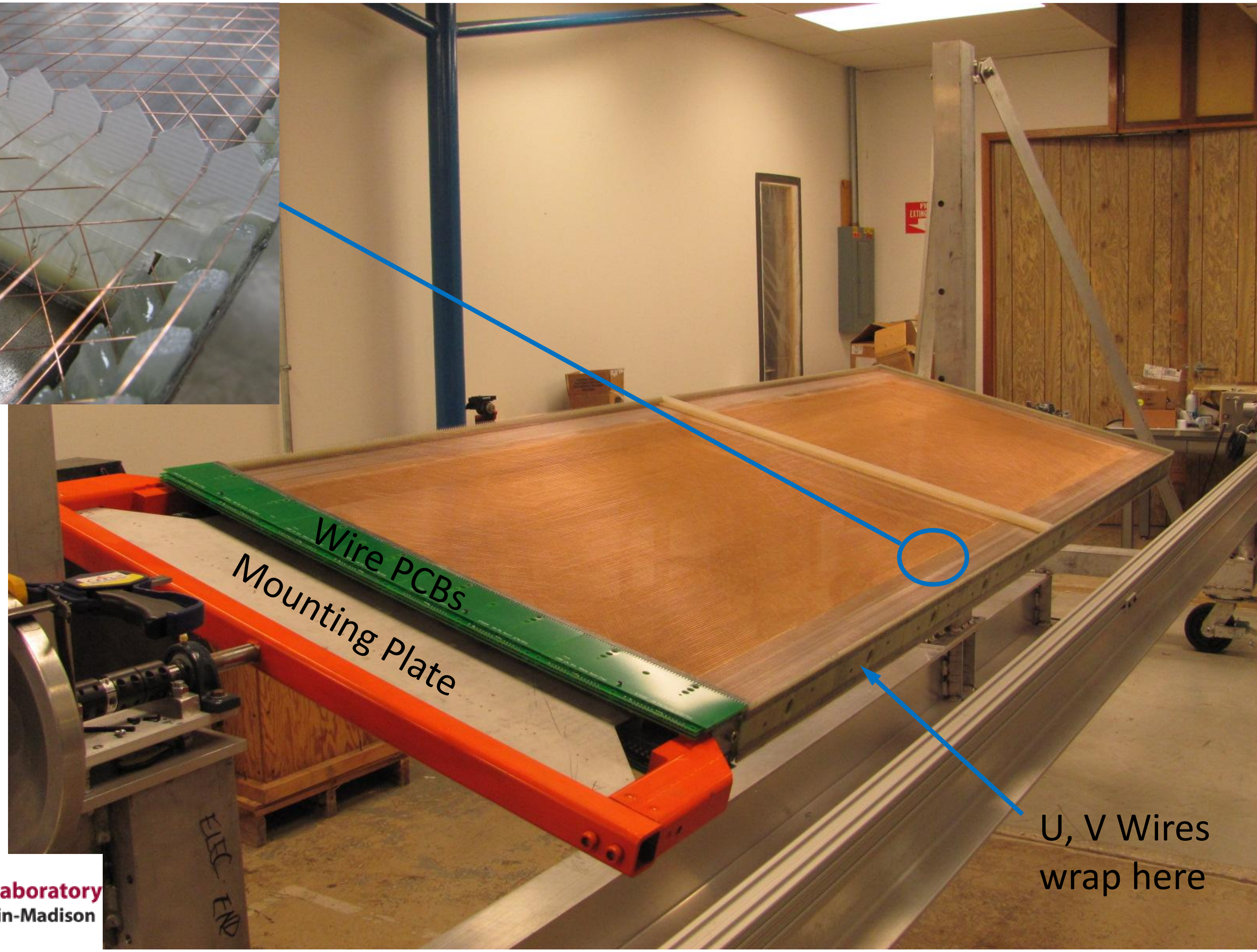


On each APA:
1120 X wires @ 4.5mm
720 U wires @ 4.9mm
720 V wires @ 5.0mm
1120 grid wires @ 4.5mm
20 front end mother boards (128ch) mounted on one end of the frame.

An alternative APA design is under development. Small (1mx2m) demonstration models are being constructed. An evaluation process will be carried out, and a decision will be made to select the baseline APA design.

APA in Fabrication at PSL, U. Wisconsin

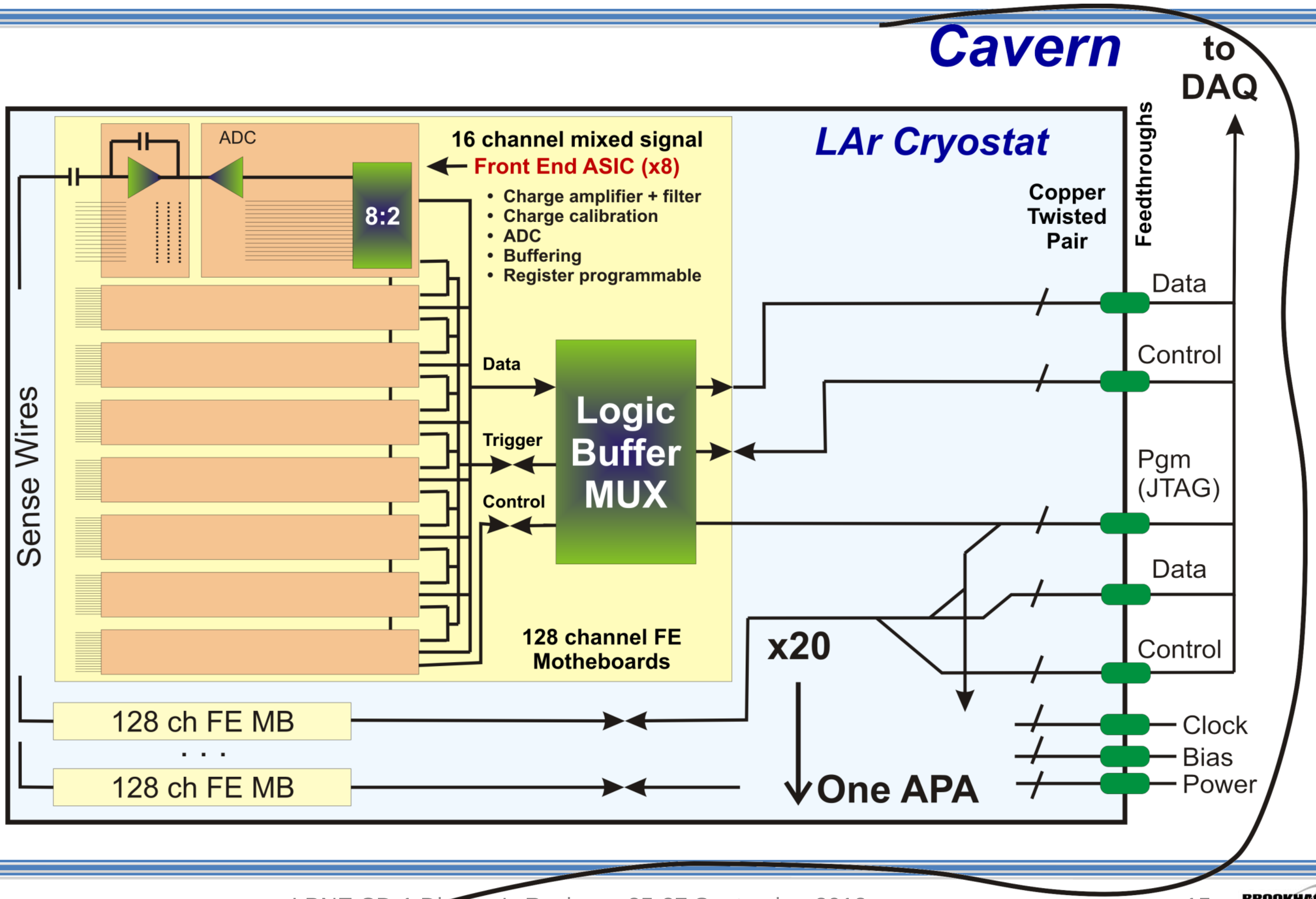




Winding wires on stainless steel frame for small prototype APA

Physical Sciences Laboratory
University of Wisconsin-Madison

LAr TPC - Cold CMOS Electronics
Block Diagram – Reference Design



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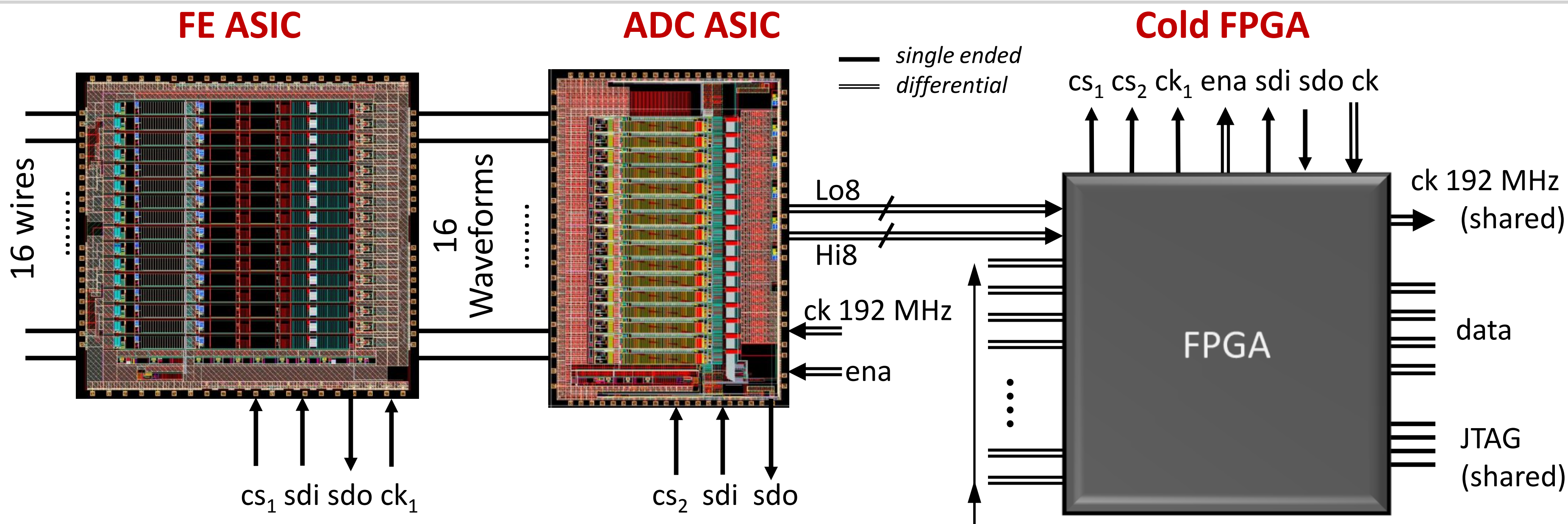
LAr TPC - Cold CMOS Electronics
Functional Diagram – Reference Design for 35t



7 additional 16 channel chains

- low-noise analog amplification
- programmable
  (gain, time constant, baseline)

- ADC 12-bit 2MS/s
- small buffer
- 2 x **8:1 multiplexing**

- **16:1 or 8:2 multiplexing**
  (total 128:1 or 64:2)
- timestamp
- compression
- zero suppression
- neighbor triggering

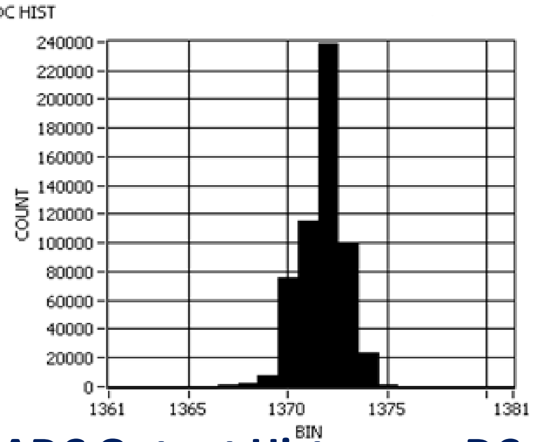
- ASIC development complete

- ASIC development in progress
- Final prototype by mid 2013

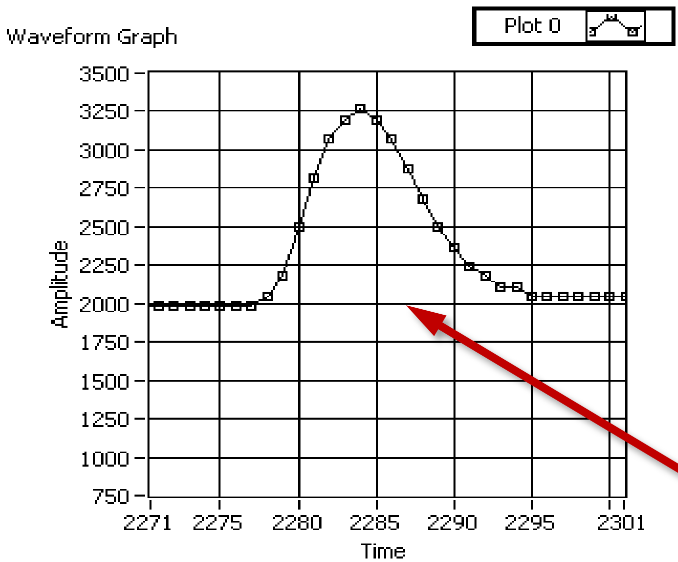
- Cold FPGA tests in progress
  (power, lifetime, driving)
- Selection by early 2013
- **Full chain test by late 2013**

Low Power CMOS ADC Designed for Operation in LAr

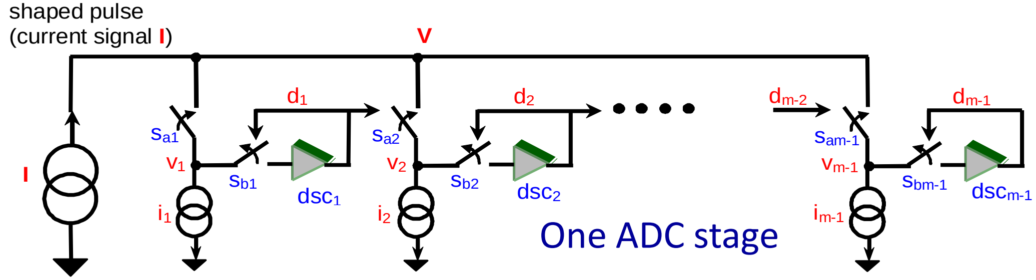
Performance at 77K



ADC Output Histogram DC



Clockless Low Power Current Mode ADC



Dual stage: 6-MSBs in 150ns, then 6-LSBs in 250ns

- Single conversion trigger per stage
- 12-bit resolution
- 2 MS/s conversion rate
- Power dissipation 3.6 mW/ch at 2 MS/s

Measured linearity

- DNL < 1.5 LSB for majority of codes
- INL ~1% of Range

Equivalent input noise measurement

- 1.27 LSB
- Effective resolution: 11.6 bits

Fabricated for normal temperature operation for SNS, see De Geronimo, et al., *IEEE Trans NSS*, **54** (2007) 541.

The ADC has been tested with an FPGA, both immersed in LN_2

LAr1: a 1 kTon LArTPC for Short Baseline Physics

Goals

- Short Baseline Oscillation Measurements
- Explore hints of sterile neutrinos
- Builds on ArgoNeut, MicroBooNE in LAr Integrated Plan
- LOI presented to FNAL PAC June 19, 2012; favorable response.
- Proposal to PAC is being prepared.

H. Chen, C. Thorn, D. Lissauer, V. Radeka, B. Yu, G. Mahler, S. Rescia, S. Duffin, Y. Li
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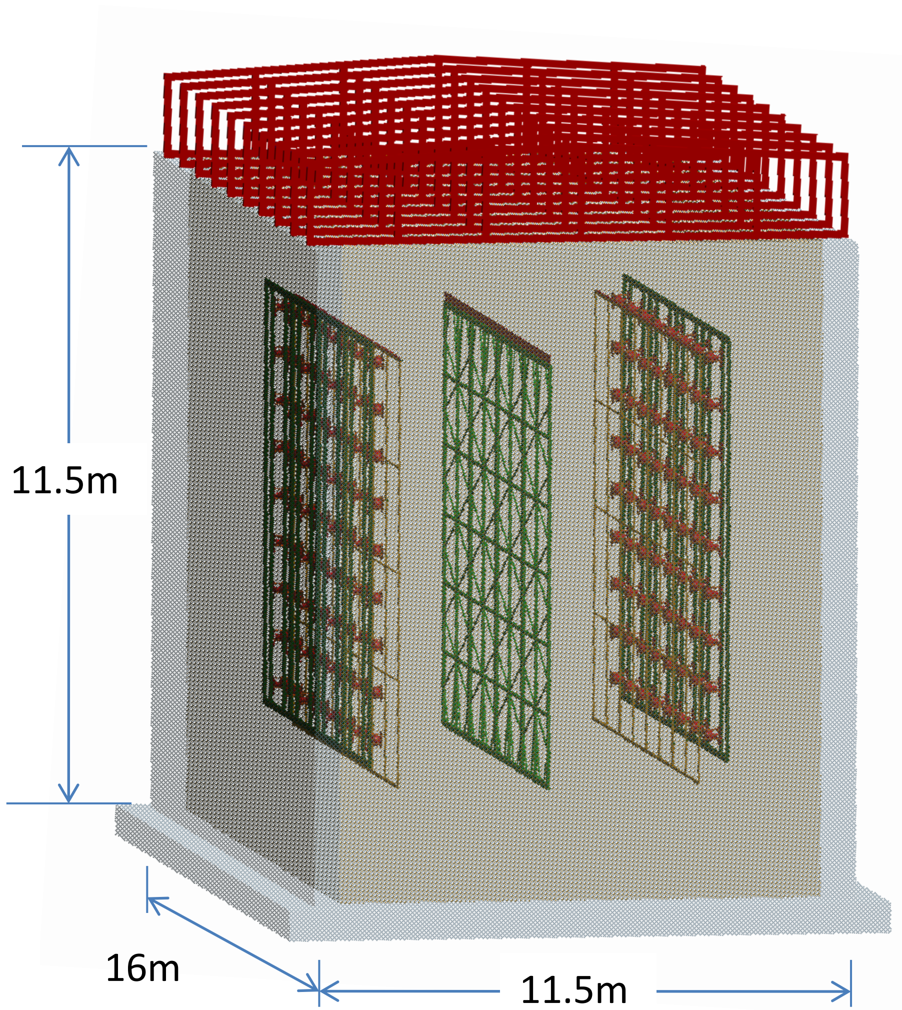
Yale University



Physics Goals

The past year in neutrino physics:

Anomalies in short baseline oscillation experiments offer hints of new physics in the neutrino sector (sterlie neutrinos?), creating lots of attention …

Hints from experiments

- LSND anamaly
- MiniBooNE anamalies (recent updates!)
- Gallex and Sage data

How to address these? (Differing philosophies …)

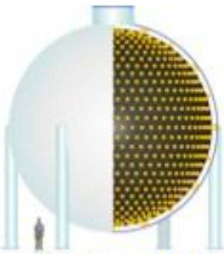
- Decay at rest sources (SNS)
- Reactor and source experiments
- Accelerator experiments

LAr1

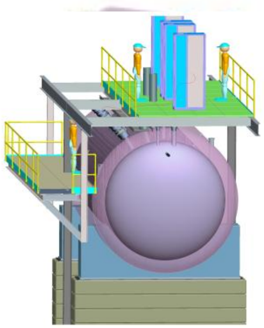
Growing interest in hints: many conferences, papers, and new ideas on how to address them

See e.g. Giunti & Laveder, arXiv:1106.4479, arXiv:1107.1452

Short Baseline Configurations on BNB

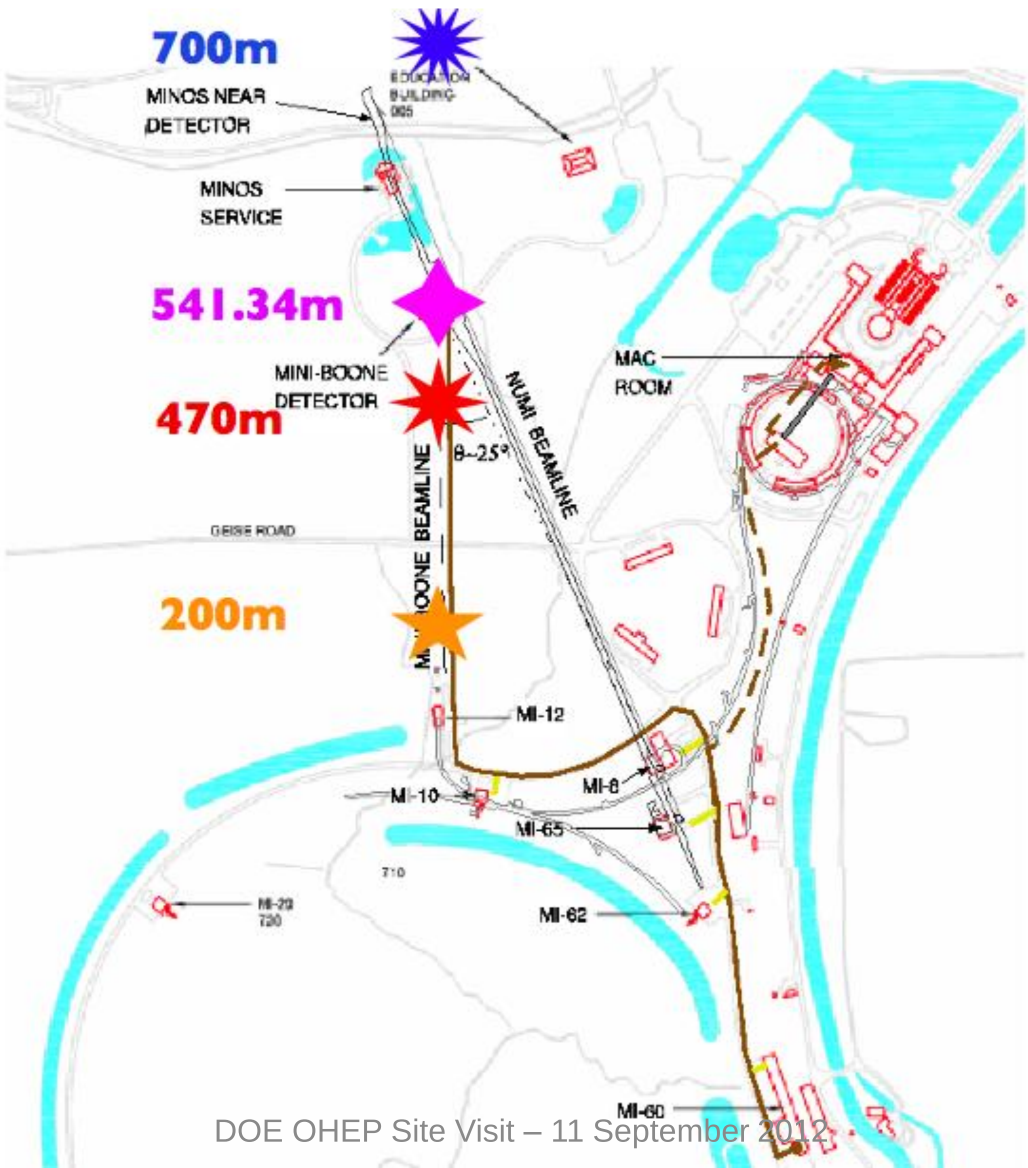


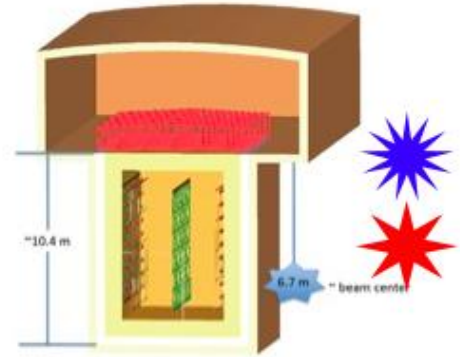
miniBooNE



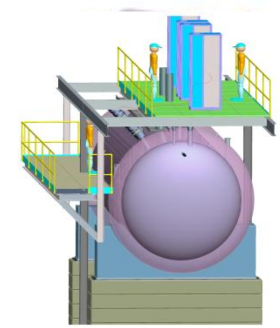
microBooNE

Phase 1





LAr1



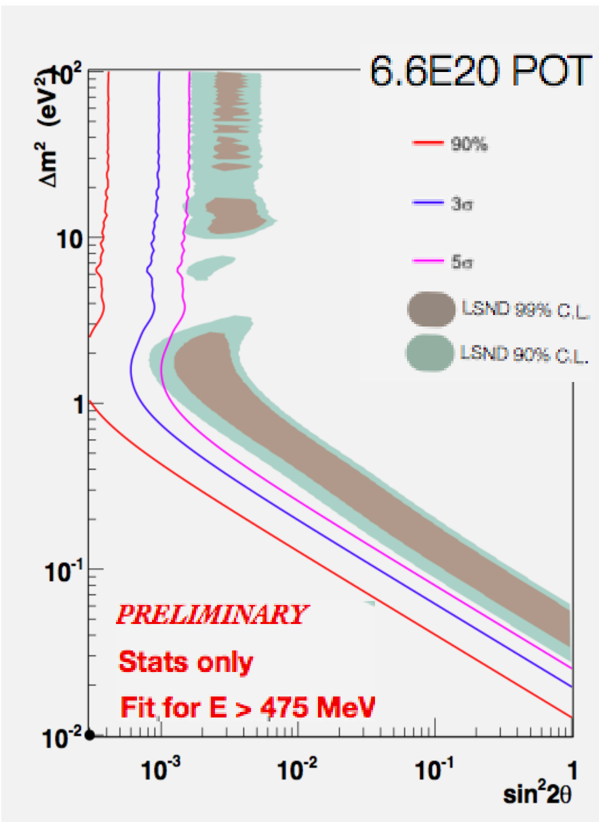
microBooNE

Phase 2

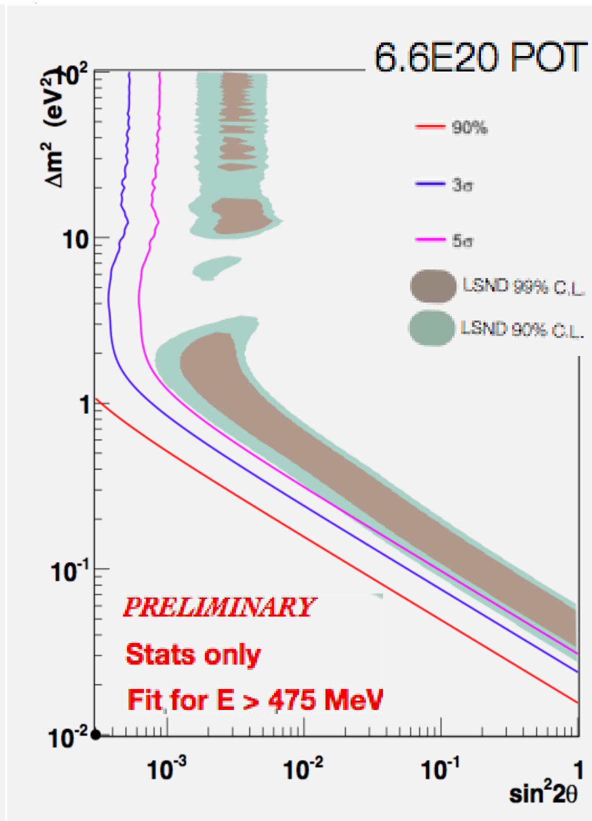
MicroBooNE + LAr1 Oscillation Sensitivities

1+1 neutrino model in neutrino mode

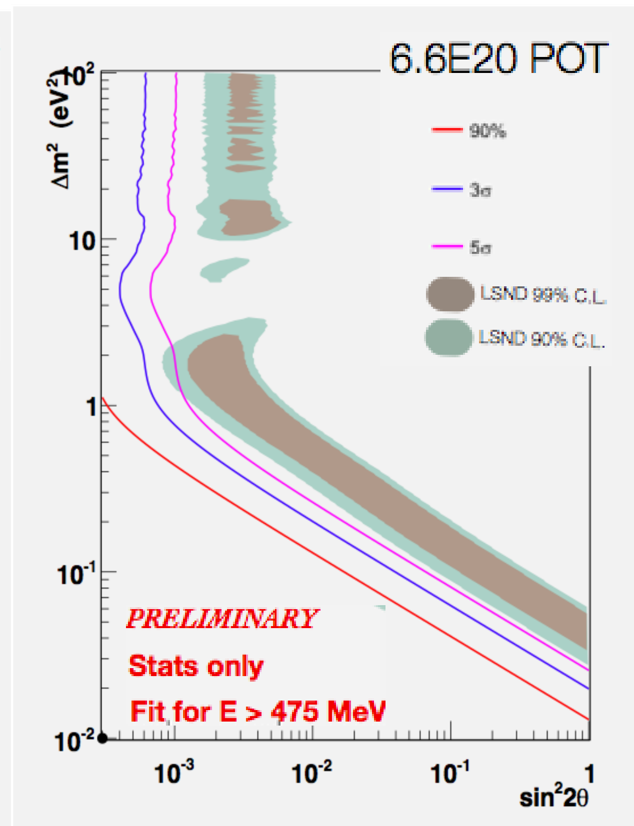
MicroBooNE @ 470m
+
LAr1 @ 700m



MicroBooNE @ (200m)
+
LAr1 @ (470m)



MicroBooNE @ 200m
+
LAr1 @ 700m



Summary

BNL is leading LAr detector development

- LAr Generic Detector R&D
- MicroBooNE Project
- LBNE Project
- LAr1 Proposal

And has been a driver of the neutrino physics that these detectors will enable